FIG.1 THE PRESENT INVENTION

SIGNAL NAME	LOGICAL EXPRESSION /FETCHING EDGE	SIGNAL SPEED (IN TERMS OF FREQUENCY)	PHASE DIFFERENCE BETWEEN CK AND DIN ±0.5*T
Din		f/2	0 1 2 3 4 5 6 7 8 9 (DATA PERIOD:T)
CK1	CK	f/2	(waveform)
CK2	CKN	f/2	(waveform)
q1	↑CK1	f/3	0 1 2 3 4 5 6 7 8
q2	↑CK2	f/3	0 1 2 3 4 5 6 7 8 9
q3	↑CK2	f/4	0 1 2 3 4 5 6
q4	↑CK1	f/4	0 1 2 3 4 5 6 7
Error1	q2 xor q3	<f/2	X1 0xor1 Y1 2xor3 4xor5
Error2	q1 xor q4	<f/2	X2 1xor2 Y2 3xor4 5xor6
Ref1	(q3 xor q4)*CK2	<f/2	0xor1 2xor3 4xor5 6xor7
Ref2	(q3 xor q4)*CK1	<f/2	1xor2 3xor4 5xor6

ERROR PULSE WIDTH:1.5*T±0.5*T

REF PULSE WIDTH:1.0*T

FIG.2 HOLMQVIST AND SUMMERS

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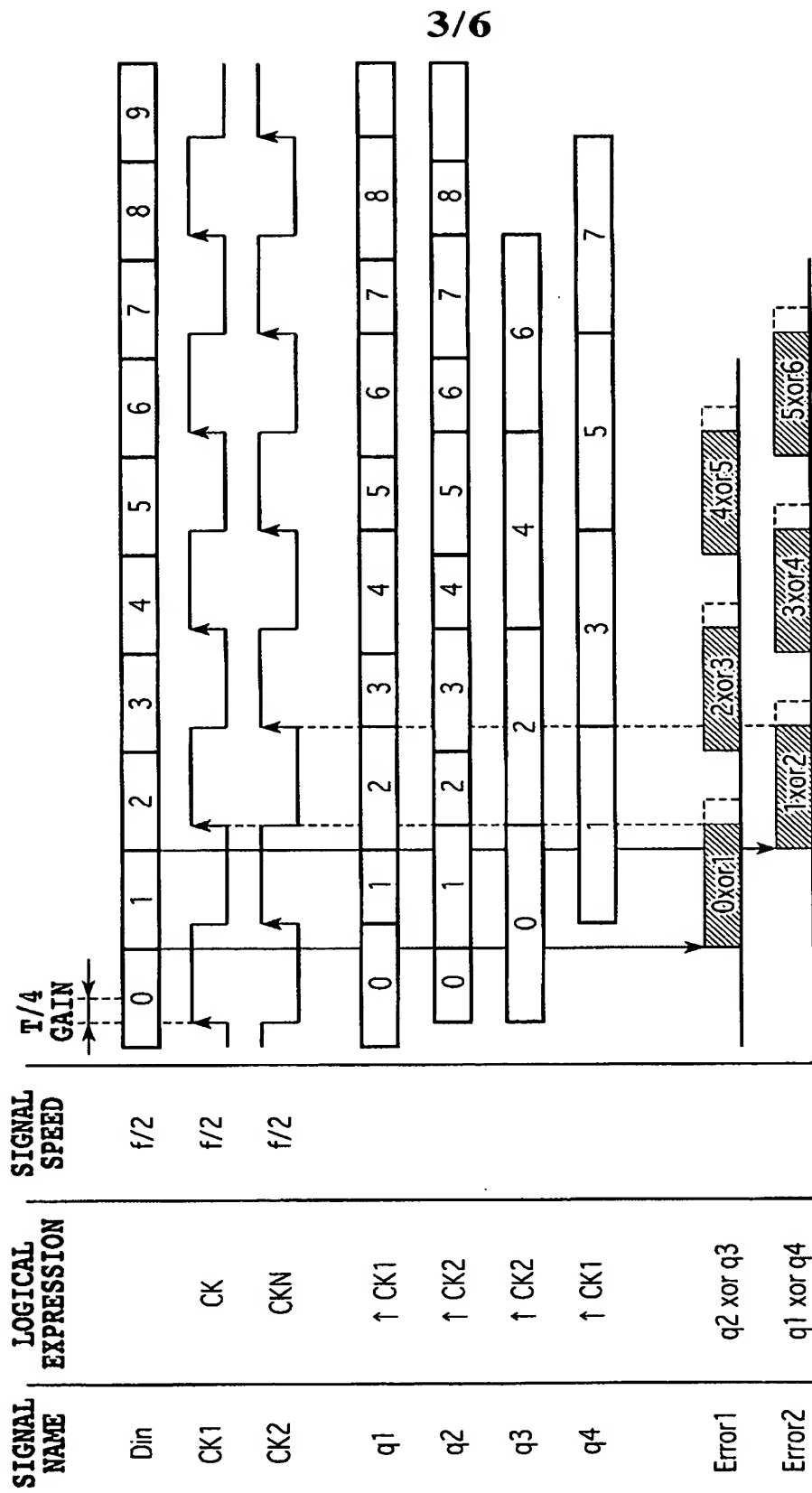| SIGNAL NAME	LOGICAL EXPRESSION	SIGNAL SPEED
(Input Signal DP		f/2
(Reference Clock CK	CK	f/2
	CKN	f/2
D-F/F 31 (701 D1	↑ CK	
D-F/F 32 (703 D3	↑ CKN	
D-F/F 33 (702 D2	↑ CKN	
D-F/F 34 (703 D4	↑ CK	
EOR 35 (705	D2 xor D3	
EOR 36 (706	D1 xor D4	

FIG.3 THE PRESENT INVENTION

SIGNAL NAME	LOGICAL EXPRESSION	SIGNAL SPEED
Din		f/2
CK1	CK	f/2
CK2	CKN	f/2
q1	↑ CK1	
q2	↑ CK2	
q3	↑ CK2	
q4	↑ CK1	
Error1	q2 xor q3	
Error2	q1 xor q4	

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FIG.4 HOLMQVIST AND SUMMERS

SIGNAL NAME	LOGICAL EXPRESSION	SIGNAL SPEED
(Input Signal DP		f/2
(Reference Clock CK	CK	f
	CKN	f
D-F/F 31 (701 D1	↑ CK	
D-F/F 32 (703 D3	↑ CKN	
D-F/F 33 (702 D2	↑ CKN	
D-F/F 34 (703 D4	↑ CK	
EOR 35 (705	D2 xor D3	
EOR 36 (706	D1 xor D4	

T/4 GAIN

Input Signal DP: 0 1 2 3 4 5 6 7 8 9

D-F/F 31: 0 1 2 3 4 5 6 7 8
D-F/F 32: 0 1 2 3 4 5 6 7 8
D-F/F 33: 0 1 2 3 4 5 6 7
D-F/F 34: 0 1 2 3 4 5 6 7

"L"

0xor1 1xor2 2xor3 3xor4 4xor5 5xor6

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FIG.5 THE PRESENT INVENTION

SIGNAL NAME	LOGICAL EXPRESSION	SIGNAL SPEED											
Din		f/2	0	1	2	3	4	5	6	7	8	9	
CK1	CK	f/2											
CK2	CKN	f/2											
q1	↑CK1		0	1	2	3	4	5	6	7	8	9	
q2	↑CK2		0	1	2	3	4	5	6	7	8	9	
q3	↑CK2		0	1	2	3	4	5	6	7			
q4	↑CK1		1	2	3	4	5	6	7				
Error1	q2 xor q3		0xor1	1xor2	2xor3	3xor4	4xor5						
Error2	q1 xor q4			1xor2	2xor3	3xor4	5xor6						

T/4 DELAY

FIG.6 HOLMQVIST AND SUMMERS

SIGNAL NAME	LOGICAL EXPRESSION	SIGNAL SPEED	
(Input Signal DP)		$f/2$	T/4 DELAY ... 0 1 2 3 4 5 6 7 8 9
(Reference Clock CK)	CK	f	
	CKN	f	
D-F/F (31 701 D1)	↑ CK		0 1 2 3 4 5 6 7 8 9
D-F/F (32 703 D3)	↑ CKN		0 1 2 3 4 5 6 7 8 9
D-F/F (33 702 D2)	↑ CKN		0 1 2 3 4 5 6 7
D-F/F (34 703 D4)	↑ CK		0 1 2 3 4 5 6 7
EOR (35 705)	D2 xor D3		0xor1 1xor2 2xor3 3xor4 4xor5 5xor6
EOR (36 706)	D1 xor D4		"L"